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EXAMINER	
FENNEMA, ROBERT E	
ART UNIT	**PAPER NUMBER**
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,823	ROCHE ET AL.	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 have been considered. Claims 1-4, 11-14, and 21-24 have been amended as per Applicant's request.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2, 9-12, 19-22, and 29-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Ronen et al. (USPN 7,171,543, herein Ronen).

4. As per Claim 1, Ronen teaches: A microprocessor comprising:

a processing unit (Figure 1, Execution Core 130);

a memory comprising a lower memory area and an extended memory area (Figure 1, Memory 120, also see Column 3, Lines 9-18, it can be addressed over 64 bits (extended), or 32 bits (lower));

an address bus connecting said processing unit to said memory (Figure 1, the bus between Memory 120 and Core 130), and comprising a lower address bus for

accessing said lower memory area and an extended address bus for accessing said extended memory area (Column 3, Lines 9-18);

means for executing instructions of an instruction set executable by said processing unit, the instruction set comprising instructions for accessing said memory (Column 3, Lines 9-18), a first instruction group comprising instructions for accessing said lower memory area, and a second instruction group distinct from the first instruction group and only comprising all of the instructions for accessing said extended memory area (Column 1, Lines 46-55. When the control flag is set, instructions from the 32-bit application will have their excess bits truncated, and tied to zero, while 64-bit applications will remain unchanged, thus allowing the 64-bit instructions to access the "extended" memory (addresses that require 17 or more bits to access. While it may appear that the control flag makes this determination, and thus the argument may be presented that a flag separates the groups, rather than the actual instruction set being partitioned into groups, it can be seen from the background of the invention that the flag is only set for 32-bit applications running in a 64-bit processor, thus the flag will only be set when a 32-bit application (using 32-bit instructions) is executing, thus, 32-bit instructions in Ronen case can only access the "lower" memory); and

means for forcing to zero an extended address transmitted by said extended address bus when executing an instruction in the first instruction group so that said lower memory area is accessed (Column 1, Lines 46-55).

5. As per Claim 2, Ronen teaches: A microprocessor according to claim 1, wherein each location in said memory is associated with a respective access address; the microprocessor further comprising means for forcing an access address of a location to be accessed to point to a location in said lower memory area when executing an instruction in the first instruction group (Column 1, Lines 46-55, 32-bit instructions are truncated and zero-extended, forcing them to the lower levels of memory).

6. As per Claims 9, 19, and 29, with Claim 9 being exemplary, Ronen teaches: A microprocessor according to claim 1, further comprising a program pointer register having a size corresponding to a size of said address bus for enabling access to a program instruction to be executed that is located at an arbitrary location in said addressable memory space (inherent in order for the system to operate).

7. As per Claims 10, 20, and 30, with Claim 10 being exemplary, Ronen teaches: a microprocessor according to claim 1, wherein said lower memory area is accessible over 16 bits and said extended memory area is accessible over 24 bits (Column 4, Lines 32-41).

8. As per Claim 11, Ronen teaches: A microprocessor comprising:

a processing unit (Figure 1, Execution Core 130)

a memory comprising a lower memory area and an extended memory area (Figure 1, Memory 120, also see Column 3, Lines 9-18, it can be addressed over 64 bits (extended), or 32 bits (lower));

an address bus connecting said processing unit to said memory (Figure 1, the bus between Memory 120 and Core 130), and comprising a lower address bus for accessing said lower memory area and an extended address bus for accessing said extended memory area (Column 3, Lines 9-18) and

a set of instructions executable by said processing unit, the set of instructions comprising a first instruction group comprising instructions for accessing said lower memory area,

a second instruction group distinct from the first instruction group and only comprising all of the instructions for accessing said extended memory area (Column 1, Lines 46-55. When the control flag is set, instructions from the 32-bit application will have their excess bits truncated, and tied to zero, while 64-bit applications will remain unchanged, thus allowing the 64-bit instructions to access the "extended" memory (addresses that require 17 or more bits to access. While it may appear that the control flag makes this determination, and thus the argument may be presented that a flag separates the groups, rather than the actual instruction set being partitioned into groups, it can be seen from the background of the invention that the flag is only set for 32-bit applications running in a 64-bit processor, thus the flag will only be set when a 32-bit application (using 32-bit instructions) is executing, thus, 32-bit instructions in Ronen case can only access the "lower" memory); and

a circuit for forcing to zero an extended address transmitted by said extended address bus when executing an instruction in the first instruction group so that said lower memory area is accessed (Column 1, Lines 46-55).

9. As per Claim 12, Ronen teaches: A microprocessor according to claim 11, wherein each location in said memory is associated with a respective access address; and the microprocessor further comprising means for forcing an access address of a location to be accessed to point to a location in said lower memory area when executing an instruction in the first instruction group (Column 1, Lines 46-55, 32-bit instructions are truncated and zero-extended, forcing them to the lower levels of memory).

10. As per Claim 21, Ronen teaches: A method for accessing a memory used by a microprocessor, the memory comprising a lower memory area and an extended memory area (Figure 1, Memory 120, also see Column 3, Lines 9-18, it can be addressed over 64 bits (extended), or 32 bits (lower)), the microprocessor comprising a processing unit (Figure 1, Execution Core 130), an address bus for connecting connected the processing unit to the memory (Figure 1, the bus between Memory 120 and Core 130), and comprising a lower address bus for accessing the lower memory area and an extended address bus for accessing the extended memory area, the method comprising (Column 3, Lines 9-18):

executing an instruction for accessing the lower memory area, the instruction belonging to an instruction set comprising a first instruction group comprising

instructions for accessing the lower memory area, and a second instruction group distinct from the first instruction group and only comprising all of the instructions for accessing the extended memory area (Column 1, Lines 46-55. When the control flag is set, instructions from the 32-bit application will have their excess bits truncated, and tied to zero, while 64-bit applications will remain unchanged, thus allowing the 64-bit instructions to access the "extended" memory (addresses that require 17 or more bits to access. While it may appear that the control flag makes this determination, and thus the argument may be presented that a flag separates the groups, rather than the actual instruction set being partitioned into groups, it can be seen from the background of the invention that the flag is only set for 32-bit applications running in a 64-bit processor, thus the flag will only be set when a 32-bit application (using 32-bit instructions) is executing, thus, 32-bit instructions in Ronen case can only access the "lower" memory);

forcing to zero an extended address transmitted by said extended address bus when executing an instruction in the first instruction group so that said lower memory area is accessed (Column 1, Lines 46-55).

11. As per Claim 22, Ronen teaches: A method according to claim 21, wherein each location in the memory is associated with a respective access address; the method further comprising forcing an access address of a location to be accessed to point to a location in the lower memory area when executing an instruction in the first instruction group (Column 1, Lines 46-55, 32-bit instructions are truncated and zero-extended, forcing them to the lower levels of memory).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 3-4, 13-14, and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ronen, in view of Suleman.

14. As per Claim 3, Ronen teaches: A microprocessor according to claim 1, further comprising at least one internal register (Column 1, Line 25), but fails to teach:

wherein the second instruction group comprises:

jump and routine call instructions at an arbitrary memory location in said memory; and

data transfer instructions between the arbitrary memory location and said at least one internal register.

Ronen teaches a system to address a memory, but does not specifically disclose all the instructions the system is capable of performing. However, Suleman teaches that in the Intel 8086 architecture, Jump (Page 14), Call (Page 16), and Move (Page 2) instructions are provided. Given that a computer needs an instruction set to run instructions, one of ordinary skill in the art would have recognized that if Ronen's invention was to be implemented in an 8086 machine in order to take advantage of the

operating system, then they would have Jump, Call, and Move instructions available to them.

15. As per Claim 4, Ronen teaches: A microprocessor according to claim 1, wherein each location in said memory is associated with a respective access address (inherent in a memory); and

The microprocessor further comprising means for maintaining an address of a jump destination location so that it points to a location in said lower memory area (Column 1, Lines 46-55, when a 32-bit application is executing (thus using 32-bit instructions), all addresses will be forced to the lower section of memory, since all extended bits are truncated away and replaced with zeros), but fails to teach:

for executing jump or routine call instructions from the first instruction group in a direct addressing mode from a location in said lower memory area.

Ronen teaches a system to address a memory, but does not specifically disclose all of the instructions the system is capable of performing. However, Suleman teaches that in the Intel 8086 architecture, Jump (Page 14), Call (Page 16), and Move (Page 2) instructions are provided. Given that a computer needs an instruction set to run instructions, one of ordinary skill in the art would have recognized that if Ronen's invention was to be implemented in an 8086 machine in order to take advantage of the operating system, then they would have Jump, Call, and Move instructions available to them.

16. As per Claim 13, Ronen teaches: A microprocessor according to claim 11, further comprising at least one internal register (Column 1, Line 25), but fails to teach:

wherein the second instruction group comprises:

jump and routine call instructions at an arbitrary memory location in said memory; and

data transfer instructions between the arbitrary memory location and said at least one internal register.

Ronen teaches a system to address a memory, but does not specifically disclose all the instructions the system is capable of performing. However, Suleman teaches that in the Intel 8086 architecture, Jump (Page 14), Call (Page 16), and Move (Page 2) instructions are provided. Given that a computer needs an instruction set to run instructions, one of ordinary skill in the art would have recognized that if Ronen's invention was to be implemented in an 8086 machine in order to take advantage of the operating system, then they would have Jump, Call, and Move instructions available to them.

17. As per Claim 14, Ronen teaches: A microprocessor according to claim 11, wherein each location in said memory is associated with a respective access address (inherent in a memory); and

said instruction set further comprises instructions for maintaining an address of a jump destination location so that it points to a location in said lower memory area (Column 1, Lines 46-55, when a 32-bit application is executing (thus using 32-bit

instructions), all addresses will be forced to the lower section of memory, since all extended bits are truncated away and replaced with zeros), but fails to teach:

executing jump or routine call instructions from the first instruction group in a direct addressing mode from a location in said lower memory area.

Ronen teaches a system to address a memory, but does not specifically disclose all the instructions the system is capable of performing. However, Suleman teaches that in the Intel 8086 architecture, Jump (Page 14), Call (Page 16), and Move (Page 2) instructions are provided. Given that a computer needs an instruction set to run instructions, one of ordinary skill in the art would have recognized that if Ronen's invention was to be implemented in an 8086 machine in order to take advantage of the operating system, then they would have Jump, Call, and Move instructions available to them.

18. As per Claim 23, Ronen teaches: A method according to claim 21, wherein the microprocessor further comprises at least one internal register (Column 1, Line 25), but fails to teach:

wherein the second instruction group comprises:

jump and routine call instructions at an arbitrary memory location in the memory; and

data transfer instructions between the arbitrary memory location and the at least one internal register.

Ronen teaches a system to address a memory, but does not specifically disclose all the instructions the system is capable of performing. However, Suleman teaches that in the Intel 8086 architecture, Jump (Page 14), Call (Page 16), and Move (Page 2) instructions are provided. Given that a computer needs an instruction set to run instructions, one of ordinary skill in the art would have recognized that if Ronen's invention was to be implemented in an 8086 machine in order to take advantage of the operating system, then they would have Jump, Call, and Move instructions available to them.

19. As per Claim 24, Ronen teaches: A method according to claim 21, wherein each location in the memory is associated with a respective access address (inherent in a memory);

the method further comprising maintaining an address of a jump destination location so that it points to a location in the lower memory area (Column 1, Lines 46-55, when a 32-bit application is executing (thus using 32-bit instructions), all addresses will be forced to the lower section of memory, since all extended bits are truncated away and replaced with zeros), but fails to teach:

for executing jump or routine call instructions from the first instruction group in a direct addressing mode from a location in the lower memory area.

Ronen teaches a system to address a memory, but does not specifically disclose all the instructions the system is capable of performing. However, Suleman teaches that in the Intel 8086 architecture, Jump (Page 14), Call (Page 16), and Move (Page 2)

instructions are provided. Given that a computer needs an instruction set to run instructions, one of ordinary skill in the art would have recognized that if Ronen's invention was to be implemented in an 8086 machine in order to take advantage of the operating system, then they would have Jump, Call, and Move instructions available to them.

20. Claims 5-8, 15-18, and 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ronen, in view of Official Notice.

21. As per Claim 5, Ronen teaches: A microprocessor according to claim 1, the microprocessor further comprising means for forcing an address and a value of a pointer that specifies access in the indirect mode so that the pointer is located in said lower memory area and points to this area (Column 1, Lines 46-55, 32-bit instructions are truncated and zero-extended to prevent access to upper levels of memory), but fails to teach:

wherein the first instruction group comprises indirect mode addressing instructions for accessing a location in said lower memory area.

While Ronen teaches a method and computer system to restrict access to certain instructions and applications, Ronen does not mention the use of indirect mode addressing. However, the concept of indirect addressing is well known in the art, and implemented in many instruction sets, and Examiner is taking Official Notice that one of ordinary skill in the art would have been able to make use of indirect addressing

instructions to run on a system such as Ronen's to address memory, and further asserts that in such a case, Ronen's truncation and zero-extension would still apply.

22. As per Claim 6, Ronen teaches: A microprocessor according to claim 1, wherein the second instruction group comprises instructions for accessing said extended memory area (Column 1, Lines 46-55, when the flag is not set (64-bit instructions are executing), access to all memory is permitted), but fails to teach:

in an indirect addressing mode (See Claim 5 rejection).

23. As per Claim 7, Ronen teaches: A microprocessor according to claim 6, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located in said lower memory area (Column 1, Lines 46-55. The 64-bit instructions have no address limitations, so can still access pointers in the lower memory area).

24. As per Claim 8, Ronen teaches: A microprocessor according to claim 6, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located within said extended memory area (Column 1, Lines 46-55. The 64-bit instructions have no address limitations, so can access pointers in the extended memory area).

25. As per Claim 15, Ronen teaches: A microprocessor according to claim 11, wherein said instruction set further comprises instructions for forcing an address and a value of a pointer that specifies access in the indirect mode so that the pointer is located in said lower memory area and points to this area (Column 1, Lines 46-55, 32-bit instructions are truncated and zero-extended to prevent access to upper levels of memory), but fails to teach:

wherein the first instruction group comprises indirect mode addressing instructions for accessing a location in said lower memory area.

While Ronen teaches a method and computer system to restrict access to certain instructions and applications, Ronen does not mention the use of indirect mode addressing. However, the concept of indirect addressing is well known in the art, and implemented in many instruction sets, and Examiner is taking Official Notice that one of ordinary skill in the art would have been able to make use of indirect addressing instructions to run on a system such as Ronen's to address memory, and further asserts that in such a case, Ronen's truncation and zero-extension would still apply.

26. As per Claim 16, Ronen teaches: A microprocessor according to claim 11, wherein the second instruction group comprises instructions for accessing said extended memory area (Column 1, Lines 46-55, when the flag is not set (64-bit instructions are executing), access to all memory is permitted), but fails to teach:

in an indirect addressing mode (See Claim 15 rejection).

27. As per Claim 17, Ronen teaches: A microprocessor according to claim 16, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located in said lower memory area (Column 1, Lines 46-55. The 64-bit instructions have no address limitations, so can still access pointers in the lower memory area).

28. As per Claim 18, Ronen teaches: A microprocessor according to claim 16, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located within said extended memory area (Column 1, Lines 46-55. The 64-bit instructions have no address limitations, so can access pointers in the extended memory area).

29. As per Claim 25, Ronen teaches: A method according to claim 21, the method further comprising forcing an address and a value of a pointer that specifies access in the indirect mode so that the pointer is located in the lower memory area and points to this area (Column 1, Lines 46-55, 32-bit instructions are truncated and zero-extended to prevent access to upper levels of memory), but fails to teach:

wherein the first instruction group comprises indirect mode addressing instructions for accessing a location in the lower memory area.

While Ronen teaches a method and computer system to restrict access to certain instructions and applications, Ronen does not mention the use of indirect mode addressing. However, the concept of indirect addressing is well known in the art, and

implemented in many instruction sets, and Examiner is taking Official Notice that one of ordinary skill in the art would have been able to make use of indirect addressing instructions to run on a system such as Ronen's to address memory, and further asserts that in such a case, Ronen's truncation and zero-extension would still apply.

30. As per Claim 26, Ronen teaches: A method according to claim 21, wherein the second instruction group comprises instructions for accessing the extended memory area (Column 1, Lines 46-55, when the flag is not set (64-bit instructions are executing), access to all memory is permitted), but fails to teach:

in an indirect addressing mode (See Claim 25 rejection).

31. As per Claim 27, Ronen teaches: A method according to claim 26, wherein in the indirect addressing mode of the extended memory area, pointers that determine an address of a memory location to be accessed are located in the lower memory area (Column 1, Lines 46-55. The 64-bit instructions have no address limitations, so can still access pointers in the lower memory area).

32. As per Claim 28, Ronen teaches: A method according to claim 26, wherein in the indirect addressing mode of the extended memory area, pointers that determine an address of a memory location to be accessed are located within the extended memory area (Column 1, Lines 46-55. The 64-bit instructions have no address limitations, so can access pointers in the extended memory area).

Response to Arguments

33. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection, as the Applicant's amendments have overcome the previous rejection, but upon a further search of the amended claims, Examiner has identified new art to apply to the claims.

Conclusion

34. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:45-6:15.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Robert E Fennema
Examiner
Art Unit 2183

RF

RICHARD L. ELLIS
PRIMARY EXAMINER